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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,121	01/22/2004	Hiroaki Nasu	9319S-000596	4193

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EXAMINER	
EGAN, SCOTT T	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/763,121	NASU, HIROAKI	
	Examiner	Art Unit	
	Scott Egan	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on December 13, 2006 and January 22, 2004 were considered by the examiner.

3. The information disclosure statement filed May 4, 2004 fails to comply with 37 CFR 1.98(a)(1), which requires the following: (1) a list of all patents, publications, applications, or other information submitted for consideration by the Office; (2) U.S. patents and U.S. patent application publications listed in a section separately from citations of other documents; (3) the application number of the application in which the information disclosure statement is being submitted on each page of the list; (4) a column that provides a blank space next to each document to be considered, for the examiner's initials; and (5) a heading that clearly indicates that the list is an information disclosure statement. The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsang et al. (US 5,900,623).

Consider **claim 1**, Tsang et al. explicitly teach:

An image-processing device (fig 4) comprising:

a solid-state image pickup element (active pixel sensor, column 4, lines 1-3) provided with a plurality of unit pixels (fig 4 demonstrates a pixel in the active pixel array), each unit pixel including a photo diode (photodiode PD, fig 4) and a plurality of transistors for detecting an optical signal (MOS transistors N1-N5, fig 4);

a circuit for changing a gate-applied voltage that changes a voltage applied to each gate of a plurality of the transistors (fig 4, each gate is connected to a voltage signal that is changed according to the timing diagram in fig 7);

a first voltage source coupled to the circuit for changing gate-applied voltage (SC, fig 4); and

a second voltage source coupled to the circuit for changing gate-applied voltage (ROW, fig 4);

wherein the circuit for changing a gate-applied voltage applies at least one of a predetermined voltage to each gate of a plurality of the transistors from the first voltage

source while in an accumulation state (the timing diagram in fig 7 shows the voltages on each transistor during integration, see ROW and SC voltages) when carriers are generated from the photo diode in response to received light, and another predetermined voltage from the second voltage source while in a reading out state when a signal in response to carriers accumulated in the accumulation state is read out (the timing diagram in fig 7 shows the voltages on each transistor during readout, see ROW and SC voltages), (see also column 7, lines 28-57).

Consider **claim 2**, Tsang et al. explicitly teach:

An image-processing device according to claim 1 further comprising:

a third voltage source coupled to the circuit for changing gate-applied voltage (RS, fig 4);

wherein the circuit for changing a gate-applied voltage applies a third predetermined voltage to each gate of a plurality of the transistors from the third voltage source while in a clearing state when residual carriers in the solid-state image pickup device are excluded from the solid-state image pickup device (the timing diagram in fig 7 show the voltages on each transistor during reset, see ROW, SC, and RS), (see also column 10, lines 12-18).

Consider **claim 3**, Tsang et al. explicitly teach:

An image-processing device according to claim 1 further comprising:

a plurality of gate voltage supplying circuits coupled to the gates of a plurality of the transistors (SC, RS, and ROW, fig 4);

wherein the changed applied voltage is applied to a plurality of the gate voltage supplying circuits from the circuit for changing a gate-applied voltage (the timing diagram in fig 7 shows the change in voltages on the transistors during different phases).

Consider **claim 4**, Tsang et al. explicitly teach:

An image-processing device according to claim 1 further comprising:

a plurality of gate voltage supplying circuits coupled to the gates of a plurality of the transistors (SC, RS, and ROW, fig 4);

wherein each of a plurality of the gate voltage supplying circuits includes the circuit for changing a gate-applied voltage (the timing diagram in fig 7 shows the change in voltages on the transistors during different phases).

Consider **claim 5**, Tsang et al. explicitly teach:

A method of image-processing that picks up an image with a solid-state image pickup element (active pixel sensor, column 4, lines 1-3) provided with a plurality of unit pixels (fig 4 demonstrates a pixel in the active pixel array), each unit pixel including a photo diode (photodiode PD, fig 4) and a plurality of transistors for detecting an optical signal (MOS transistors N1-N5, fig 4), the method comprising:

applying a predetermined voltage to each gate of a plurality of the transistors from a first voltage source while in an accumulation state when carriers are generated from the photo diode in response to received light (the timing diagram in fig 7 shows the change in voltages on each transistor during integration, see ROW and SC voltages); and

applying a predetermined voltage to each gate of a plurality of the transistors from a second voltage source while in a reading out state when a signal in response to carriers accumulated in the accumulation state is read out (the timing diagram in fig 7 shows the change in voltages on each transistor during readout, see ROW and SC voltages).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsang et al. (US 5,900,623).

Consider **claim 6**, Tsang et al. explicitly teach:

A solid-state image pickup device (fig 4) comprising:

a solid-state image pickup element (active pixel sensor, column 4, lines 1-3) provided with a plurality of unit pixels (fig 4 demonstrates a pixel in the active pixel array), each unit pixel including a photo diode (photodiode PD, fig 4) and a plurality of transistors for detecting an optical signal (MOS transistors N1-N5, fig 4);

a circuit for changing a gate-applied voltage that changes a voltage applied to each gate of a plurality of the transistors (fig 4, each gate is connected to a voltage signal that is changed according to the timing diagram in fig 7); and

a regulator that produces a first voltage and a second voltage;

wherein the circuit for changing gate-applied voltage applies at least one of the first voltage output from the regulator to each gate of a plurality of the transistors while in an accumulation state when carriers are generated from the photo diode in response to received light (the timing diagram in fig 7 shows the voltages on each transistor during integration, see ROW and SC voltages), and the second voltage output from the regulator to each gate of a plurality of the transistors while in a reading out state when a signal in response to carriers accumulated in the accumulation state is read out (the timing diagram in fig 7 shows the voltages on each transistor during readout, see ROW and SC voltages), (see also column 7, lines 28-57).

However, Tsang et al. does not explicitly teach the use of a regulator that produces several voltages, which are then used on the transistors.

Official Notice is taken that both the concept and the advantages of providing a regulator to provide different voltage values to different destinations from one source is well known and expected in the art. It would have been obvious to one of ordinary skill

in the art at the time the invention was made to include a regulator in the active pixel sensor found in Tsang et al. as regulators are known to stabilize a desired voltages on multiple paths.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Bock (US 2004/0036784) teaches a high dynamic range pixel, which includes three phases of operation, accumulation, read-out and reset. Figure 4 shows the gate-applied voltages, which are changed during the phases.

b. Beiley (US 6,243,134) teaches a CMOS image sensor with accumulation, readout and reset. Figure 1 shows the gate-applied voltages, which are changed during each phase.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Egan whose telephone number is (571) 270-1452. The examiner can normally be reached on Monday-Friday 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SE

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER